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portions 205, 215. In some embodiments, ground traces 230, 235 lie on either side of the neck down portions 205, 215 on the same layer of the circuit board 225. A ground plane 240 may lie above or below the signal lines 200, 210 on another layer of the circuit board. --

In the claims:

Claims 2, 9 and 15 have been cancelled.

Claims 1, 4-6, 8-14, 16-20 have been amended as follows:

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-- 1. (Amended) A computer system comprising:

a processor;

a memory unit configured to store data used by the processor;

a memory control unit configured to manage data flowing into and out of the memory unit;

a circuit board having multiple layers and comprising:

a first signal line, formed on a first layer of the circuit board and connected between a first connection on the memory unit and the memory control unit; and

a second signal line also formed on the first layer of the circuit board and connected to the first connection on the memory unit, a first portion of the second signal line substantially parallel to a first portion of the first signal line, a second portion of the second signal line at an acute angle relative to a second portion of the first signal line,

wherein said layer defines a non-grounded gap between said first and second lines

4. (Amended) The system of claim 1, wherein the first signal line and the portion of the second signal line that is routed substantially parallel to the first signal line have substantially equal widths.

5. (Amended) The system of claim 4, wherein the first signal line and the portion of the second signal line that is routed substantially parallel to the first signal line are separated by a distance approximately equal to said widths.

6. (Amended) The system of claim 5, wherein the widths of the lines and the distance separating the lines are each about 5 mils.

8. (Amended) A method for use in routing signals between a memory unit and a memory control unit, the method comprising:

delivering a first signal over a first signal line formed on a selected layer of a circuit board and connected between the memory control unit and on the memory unit;

delivering a second signal over a second signal line formed on the selected layer of the circuit board and connected to the first connection of the memory unit, a first portion of the second signal line formed substantially parallel to a first portion of the first signal line, a second portion of the second signal line formed at an acute angle relative to a second portion of the first signal line; and

separating said first and second signal lines without a ground connection therebetween.

10. (Amended) The method of claim 8, further comprising delivering another signal to said memory control unit on another

layer of the circuit board over portions of the first and second signal lines that are not separated by any conductive traces.

11. (Amended) The method of claim 8, wherein delivering the first signal and the second signal include delivering the signals over portions of the first and second signal lines that have substantially equal widths.

12. (Amended) The method of claim 11, wherein delivering the first signal and the second signal include delivering the signals over portions of the first and second signal lines that are separated by a distance substantially[approximately] equal to their widths.

13. (Amended) The method of claim 12, wherein delivering the first signal and the second signal include delivering the signals over portions of the first and second signal lines that are about 5 mils wide and that are separated by a distance of about 5 mils.

14. (Amended) A method for use in manufacturing a computer system, the method comprising:

forming a multiple-layer circuit board with first and second signal lines on a selected layer of the board;

connecting a memory unit to the board such that a first connection on the memory unit connects to the first and second signal lines;

affixing a memory control unit to the board such that the memory control unit connects to at least the first signal line;

forming a first portion of the second signal line to be substantially parallel to a first portiong of the first signal line; and

forming a second portion of the second signal line to be at an acute angle relative to a second portion of the first signal line.

16. (Amended) The method of claim 14, further comprising forming the first and second signal lines such that no conductive trace lies between the first signal line and the first portion of the second signal line that is routed roughly parallel to the first signal line.

17. (Amended) The method of claim 16, further comprising forming the first signal line and the first portion of the second signal line that is routed roughly parallel to the first signal line to have substantially equal widths.

18. (Amended) The method of claim 17, further comprising forming the first signal line and the first portion of the second signal line that is routed substantially parallel to the first signal line to be separated by a distance approximately equal to their widths.

19. (Amended) The method of claim 18, further comprising forming the signal lines such that the widths of the lines and the distance separating the lines are all about equal to 5 mils.

20. (Amended) A circuit board for use in a computer system comprising:

a memory unit;

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a memory control unit; and

a data bus connecting the memory control unit to the memory unit and comprising:

a first signal line formed on a selected layer of the circuit board and connected to the memory control unit and to a first connection on the memory unit; and

a second signal line formed on the selected layer of the circuit board and also connected to the first connection on the memory control unit, a first portion of the second signal line substantially parallel to a first portion of the first signal line, a second portion of the second signal line at an acute angle relative to a second portion of the first signal line,

wherein said selected layer defines a non-grounded gap between said first and second lines. --

Please add claims 21 and 22.

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-- 21. The circuit board of claim 20, wherein the first connection comprises a pin connection.

22. (New) The computer system of claim 1, wherein the first connection on the memory unit comprises a pin connection. --

In the drawings:

Please substitute corrected drawings for FIGS. 1-3. The corrections on the drawings are marked in red.